

Specification


OSFP 800G SR8 Transceiver

(Preliminary)



TES-K18HE-8CZ

Ordering Information

Model Name	TES-K18HE-8CZ	Note
Voltage	3.3V	
Device type	850nm VCSEL	
Temperature	0°C~+70°C	
Distance	60m (OM3) / 100m (OM4)	
Optical interface	MPO16 connector	
Latch Color	Beige 	

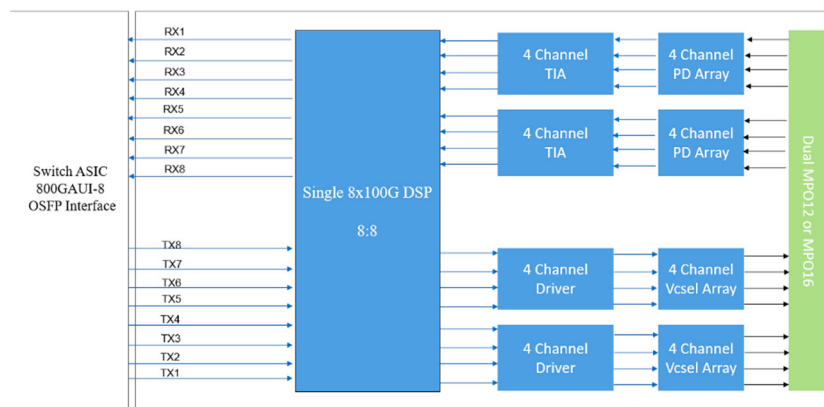
■ Features

- 8-channels of 100G-PAM4 electrical modulation
- 8-channel 100G-PAM4 optical modulation
- Finned-top OSFP for air-cooled switches
- 8 channel VCSEL arrays and 8 channels PIN photo detector arrays
- Maximum reach : 60m / 100m via OM3/ OM4 fiber
- MPO16 APC optical connectors
- Single 3.3V power supply
- Class 1 laser safety
- Hot pluggable OSFP form factor
- Complaint to OSFP Module Specification Rev 5.0
- Compliant with CMIS 5.2
- Compliant with IEEE 802.3db
- Compliant with IEEE 802.3ck
- Power Consumption <16W
- Case temperature operating range 0°C to +70°C

■ Applications

- 800GBASE-SR8 800G Ethernet
- Data Center and Enterprise Networking

■ Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Maximum Supply Voltage	Vcc	-0.5		3.6	V	
Storage Temperature	Ts	-40		85	°C	
Relative Humidity (no-condensation)	RH	15		85	%	
Case Operating Temperature	Top	0		70	°C	
Receiver Damage Threshold, per Lane		5			dBm	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Operating Case Temperature	Top	0		70	°C	
Supply Current per end	Icc			5.1	A	
Total Power Consumption				16	W	
Bit Rate				850	Gbps	
Case Temperature	Top	0		70	°C	
Link Distance (OM4)				100	m	
Link Distance (OM3)				60	m	
Pre FEC Bit Error Ratio				2.4E-4		
Post FEC Bit Error Ratio				1E-12		
I2C Clock Frequency				1000	kHz	

Notes:

1. Under condition of 3.465V operating supply voltage, and 70°C case temperature.

Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Transmitter (each lane)						
Differential Peak-to-Peak input Voltage tolerance	TP1a	750			mV	
Differential termination mismatch	TP1			10	%	
Eye height		10			mV	
Differential to common-mode return loss, RLcd	TP1	IEEE802.3ck Equation (120G-1)				
Vertical eye closure				12	dB	
Effective return loss, ERL	TP1	7.3			dB	
Transition Time		10			ps	
Receiver (each lane)						
Differential data output swing		300		900	mVpp	
Differential Termination Mismatch	TP4			10	%	
Eye Height (EH)	TP4	15			mV	
Vertical Eye Closure (VEC)	TP4			12	dB	
Common-mode to differential return loss, RLdc	TP4	IEEE 802.3ck Equation (120G-1)				
Effective Return Loss (ERL)	TP4	8.5			dB	
Transition Time	TP4	8.5			ps	

Electrical Specification for Low Speed Signal

Parameter	Symbol	Min	Max	Unit
Module Output SCL and SDA	VOL	0	0.4	V
	VOH	VCC-0.5	VCC+0.3	V
Module Input SCL and SDA	VIL	-0.3	VCC*0.3	V
	VIH	VCC*0.7	VCC+0.5	V

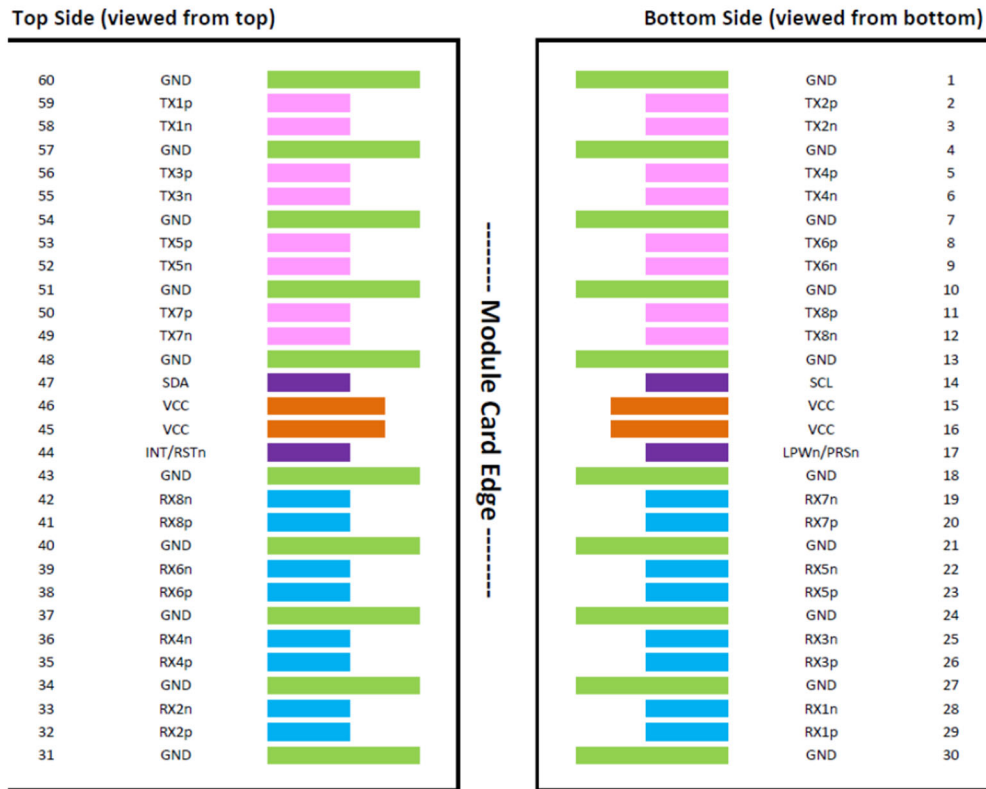
Optical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Transmitter						
Center Wavelength	λ	840	860	868	nm	1
RMS spectral width	σ			0.6	nm	
Average launch power, each lane	P_{AVG}	-1		4.0	dBm	
Optical Power OMA, each Lane, max	P_{OMA}	3.5			dBm	
OMA _{outer} , each lane		Max [-2.6, max (TECQ, TDECQ) -4.4]			dBm	
OMA _{min}						
Transmitter and Dispersion penalty, each lane	TDECQ			4.4	dB	
Transmitter eye closure for PAM4 (TECQ), each lane	TECQ			4.4	dB	
Average Launch Power of OFF Transmitter, each lane	P_{off}	-	-	-30	dBm	
Extinction Ratio, each lane		2.5			dB	
Transmitter power excursion, each lane				2.3	dBm	
Optical Return Loss Tolerance	ORLT			14	dB	
Encircled flux _b		$\geq 86\%$ at 19 μ m $\leq 30\%$ at 4.5 μ m				2
Receiver						
Center Wavelength	λ	842	850	948	nm	
Damage Threshold, average optical power, each lane	AOPD	5	-	-	dBm	
Average receive power, each lane	AOPR	-6.4	-	4.0	dBm	
Receive Power (OMA _{outer}), each lane	OMA-R	-	-	3.5	dBm	
Receiver Reflectance	RR			-15	dB	
Receiver sensitivity (OMA _{outer}), each lane	SOMA	RX = max (-4.6, TECQ -6.4)			dBm	3
Stressed receiver sensitivity (OMA _{outer}), each lane	SRS			-2.0	dBm	
RX LOS Assert		-15			dBm	
RX LOS De-assert				-7.5	dBm	
RX LOS Hysteresis		0.5			dB	

Notes:

1. Defined according to the performance of the laser used
2. Measured into type A1a.2 or type A1a.3, or A1a.4, 50 μ m fiber, in accordance with IEC 61280-1-4
3. Receiver sensitivity is informative and is defined for a transmitter with a value of TECQ. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre FEC

Module Pad Assignments and Descriptions

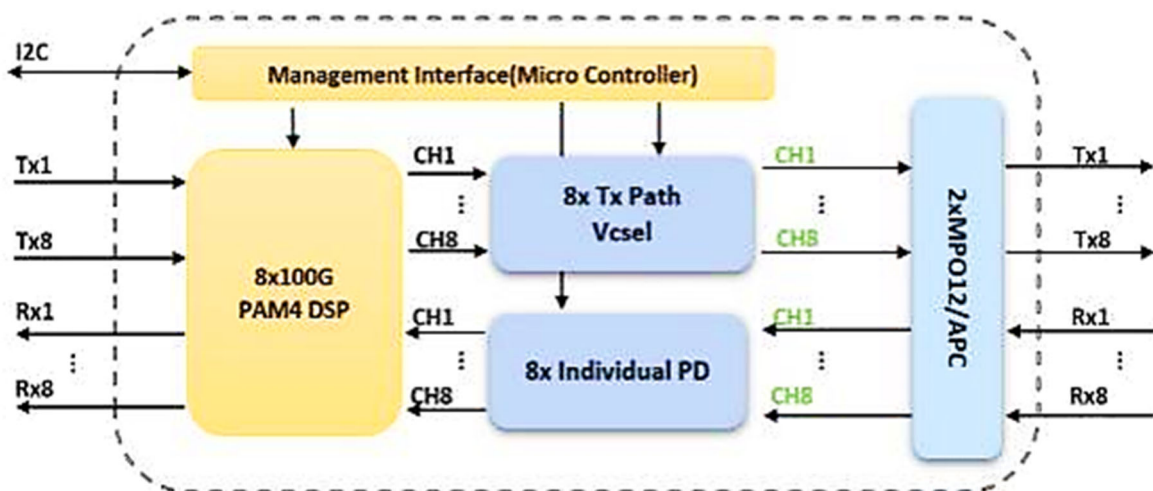


Pin	Logic	Symbol	Description
1	GND	GND	Ground
2	CML-I	Tx2p	Transmitter Non-Inverted Data Input
3	CML-I	Tx2n	Transmitter Inverted Data Input
4	GND	GND	Ground
5	CML-I	Tx4p	Transmitter Non-Inverted Data Input
6	CML-I	Tx4n	Transmitter Inverted Data Input
7	GND	GND	Ground
8	CML-I	Tx6p	Transmitter Non-Inverted Data Input
9	CML-I	Tx6n	Transmitter Inverted Data Input
10	GND	GND	Ground
11	CML-I	Tx8p	Transmitter Non-Inverted Data Input
12	CML-I	Tx8n	Transmitter Inverted Data Input

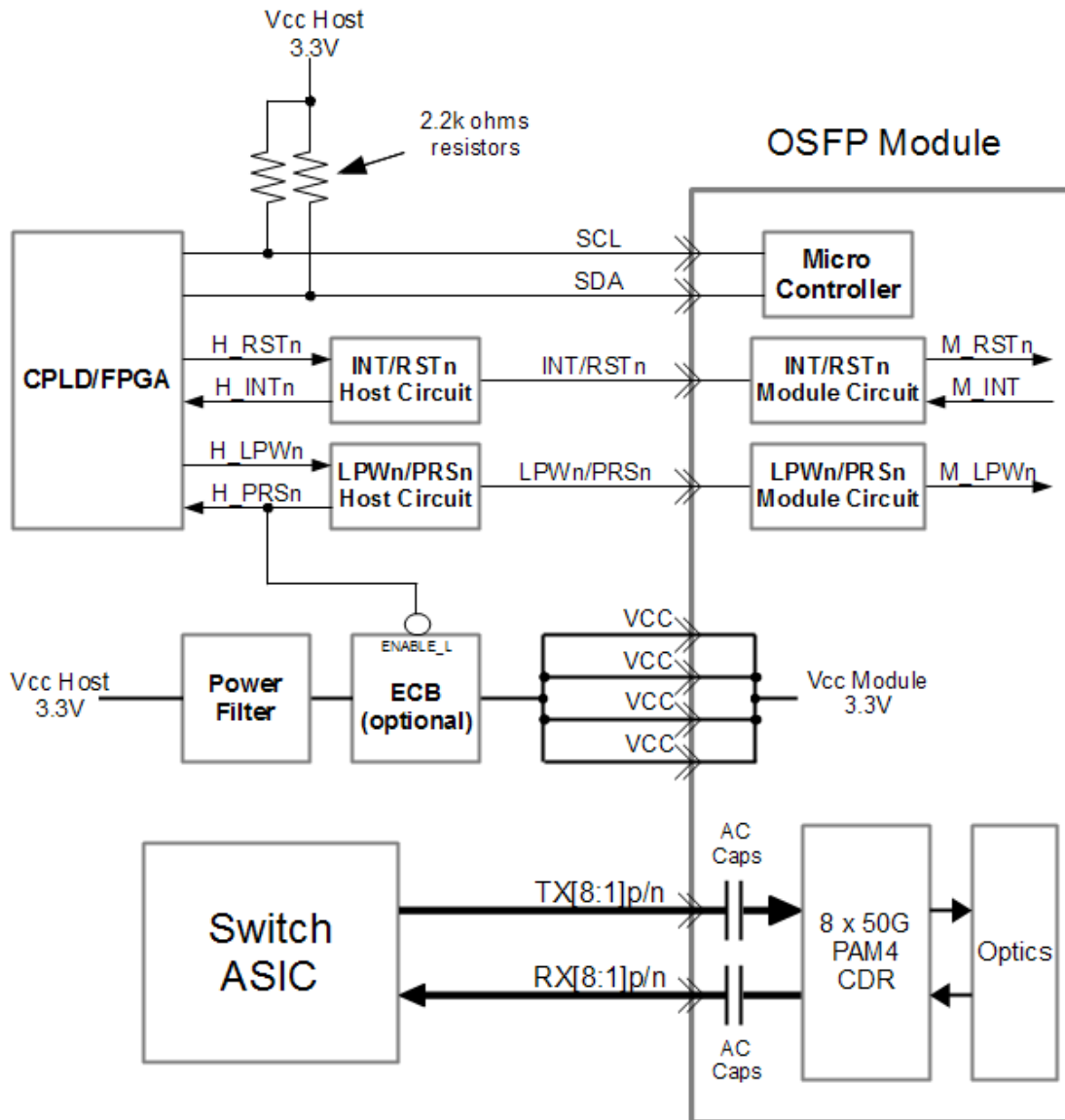
13	GND	GND	Ground
14	LVCOMS	SCL	2-wire Serial Interface Clock
15	VCC	VCC1	+3.3V Power Supply
16	VCC	VCC1	+3.3V Power Supply
17	Muti-Level	LPWn/PRSn	Low-Power Mode / Module Present
18	GND	GND	Ground
19	CML-O	Rx7n	Receiver Inverted Data Output
20	CML-O	Rx7p	Receiver Non-Inverted Data Output
21	GND	GND	Ground
22	CML-O	Rx5n	Receiver Inverted Data Output
23	CML-O	Rx5p	Receiver Non-Inverted Data Output
24	GND	GND	Ground
25	CML-O	Rx3n	Receiver Inverted Data Output
26	CML-O	Rx3p	Receiver Non-Inverted Data Output
27	GND	GND	Ground
28	CML-O	Rx1n	Receiver Inverted Data Output
29	CML-O	Rx1p	Receiver Non-Inverted Data Output
30	GND	GND	Ground
31	GND	GND	Ground
32	CML-O	Rx2p	Receiver Non-Inverted Data Output
33	CML-O	Rx2n	Receiver Inverted Data Output
34	GND	GND	Ground
35	CML-O	Rx4p	Receiver Non-Inverted Data Output
36	CML-O	Rx4n	Receiver Inverted Data Output
37	GND	GND	Ground
38	CML-O	Rx6p	Receiver Non-Inverted Data Output
39	CML-O	Rx6n	Receiver Inverted Data Output
40	GND	GND	Ground
41	CML-O	Rx8p	Receiver Non-Inverted Data Output
42	CML-O	Rx8n	Receiver Inverted Data Output
43	GND	GND	Ground
44	Muti-Level	INT/RSTn	Module Interrupt / Module Reset

45	VCC	VCC1	+3.3V Power Supply
46	VCC	VCC1	+3.3V Power Supply
47	LVCMOS	SDA	2-wire Serial Interface Data
48	GND	GND	Ground
49	CML-I	Tx7n	Transmitter Inverted Data Input
50	CML-I	Tx7p	Transmitter Non-Inverted Data Input
51	GND	GND	Ground
52	CML-I	Tx5n	Transmitter Inverted Data Input
53	CML-I	Tx5p	Transmitter Non-Inverted Data Input
54	GND	GND	Ground
55	CML-I	Tx3n	Transmitter Inverted Data Input
56	CML-I	Tx3p	Transmitter Non-Inverted Data Input
57	GND	GND	Ground
58	CML-I	Tx1n	Transmitter Inverted Data Input
59	CML-I	Tx1p	Transmitter Non-Inverted Data Input
60	GND	GND	Ground

Transceiver Block Diagram

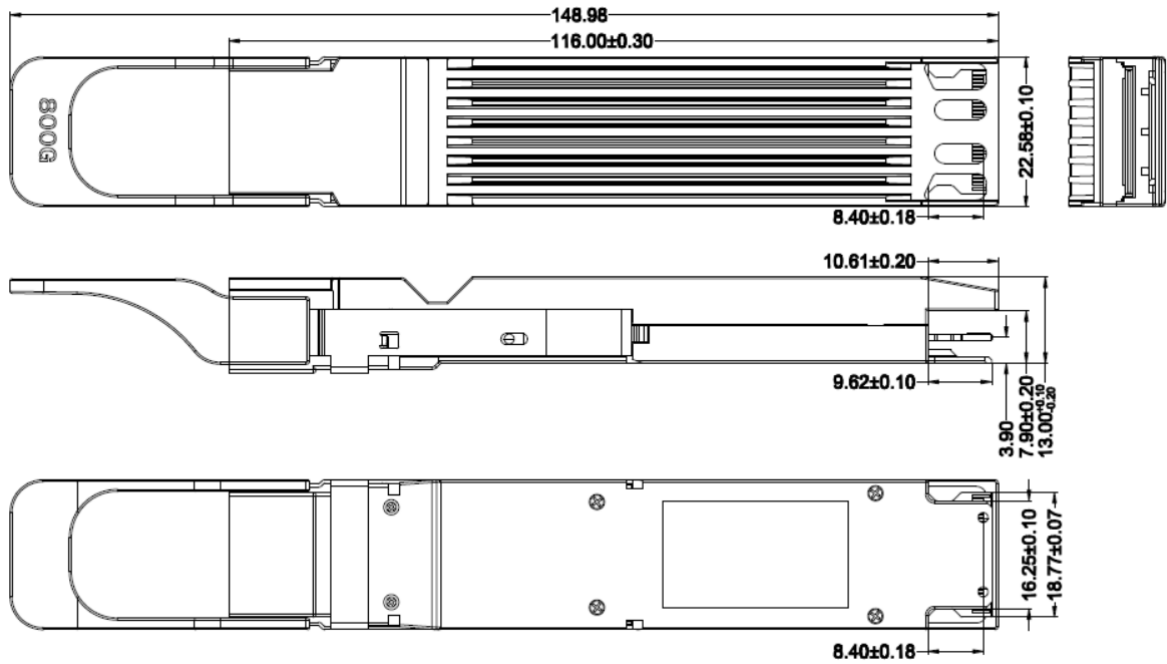


OSFP Host Board and Module Block Diagram

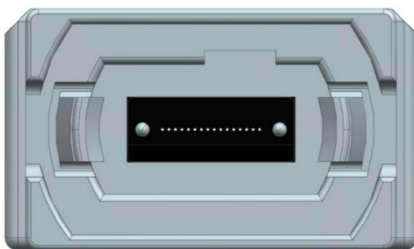


Mechanical Design Diagram

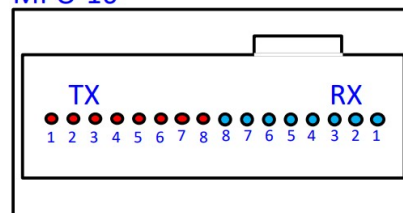
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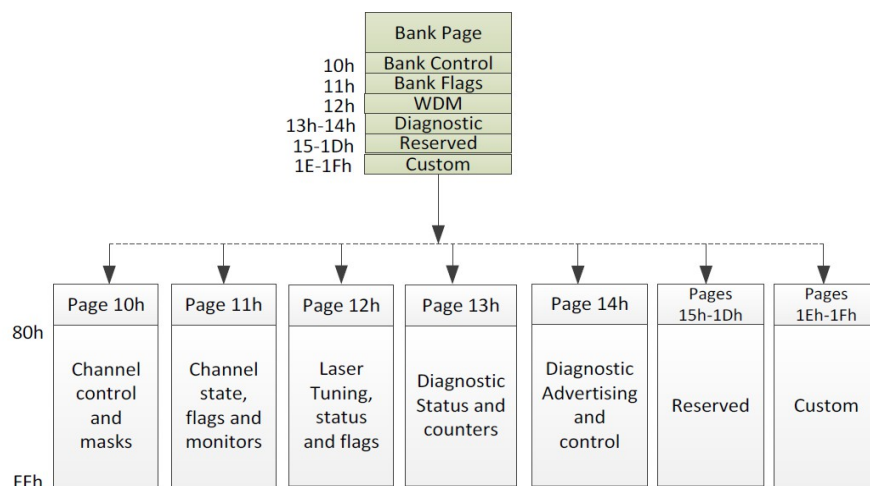
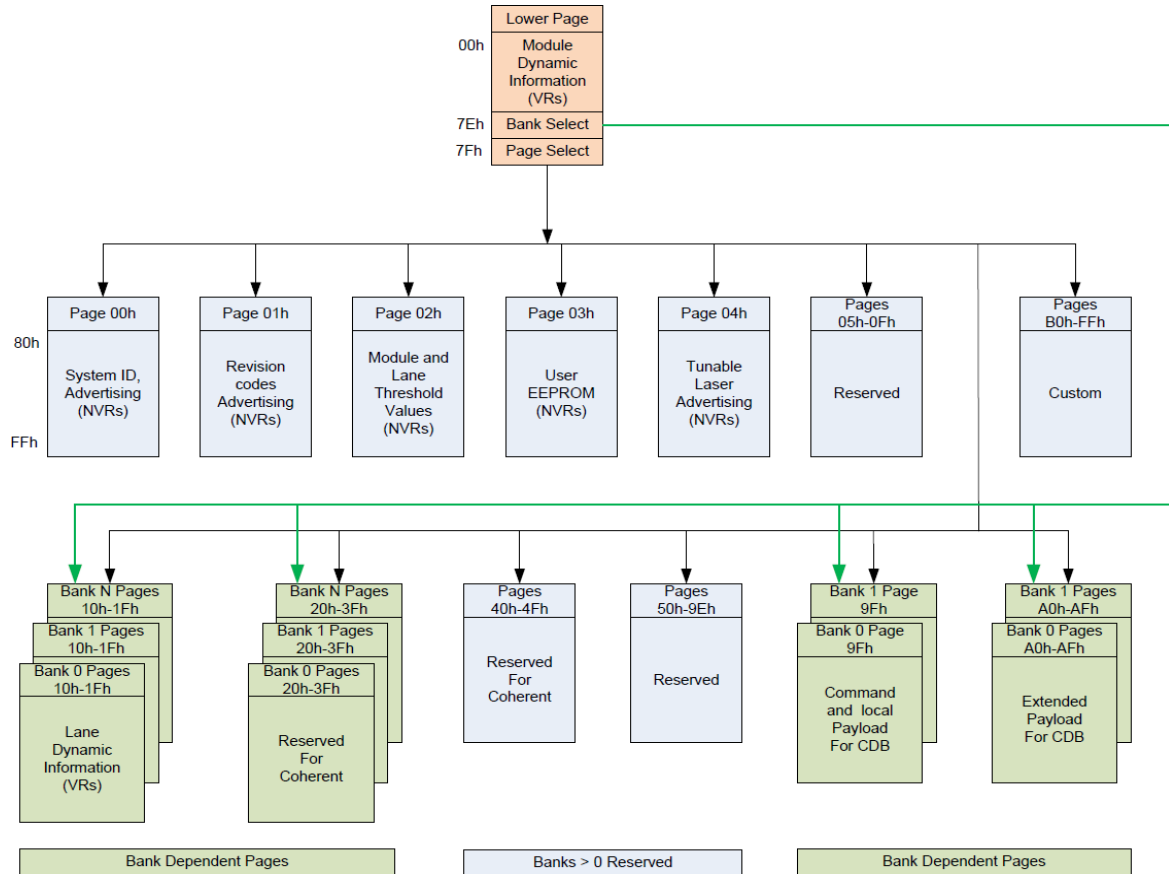
Optical Interface



MPO-16



CMIS Memory Map



■ Contact Information

Formerica OptoElectronics Inc.

5F-11, No.38, Taiyuan St., Zhubei City,
Hsinchu County 30265, Taiwan

Tel: +886-3-5600286

Fax: +886-3-5600239

inquiry@formericaoe.com

www.formericaoe.com

■ Revision History

Date	Version	Description
3/22/2024	0.1	Preliminary release